REMARKS

The rejection under 35 USC 103 for obviousness from the cited Ichinose, et al. and Ishimi patents is traversed by adding the oscillator to claim 1 and limiting claim 1 to only one high frequency clock region. Because the object of the invention is to provide more clocks than one high frequency clock region can provide, it would be obvious to provide more multiple high frequency clock regions to achieve more clocks, but this does not make obvious the claimed delay-lock-loop way of getting more clocks out of only one high frequency clock region.

The real-time clock module 2 of the Ichinose, et al. patent functions as a baseband clock generator that generates a 32.768 KHz baseband clock signal, and phase lock loops 11, 12, 13, 14, 15 and 16 are distributed in the circuit board of system 4 for respectively cooperating with various IC components. Therefore, the patent teaches the obvious way of getting more clocks from more high frequency clock regions and not the claimed way of more clocks from only one high frequency clock region.

In an alternative view, the real-time clock module 2 is only an oscillator (baseband clock generator), as now added separately to claim 1, and not the distinctly claimed low frequency clock region well-defined in Claim 1.

The addition to the rejection of the Ishimi patent for disclosing a low frequency clock 21 including a phase lock loop 40 and at least one delay lock loop 41, at least because 41 is not a loop. In the Ishimi patent 41 is a "... phase locked circuit 41 (hereinafter it is also referred to as a phase locked section 41)" as at column 6, lines 31-33, and not a loop. As a result, it can only produece as many clocks as it has combinations digital delay lines, i.e., four in Fig. 2, and not the variables of the claimed delay lock loop.

Specifically, as also shown in Fig. 2, it does not have feedback, as specifically claimed in claim 4.

Therefore, the combination of the patents does not make the claimed invention obvious and reconsideration and allowance are requested.

Respectfully submitted,

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1. (amended) A universal clock generator comprising:

a only one high frequency clock region for generating high frequency clocks; and

a low frequency clock region connecting to the high frequency clock region including:

(a) a phase lock loop for generating low frequency clocks, and

(b) at least one delay lock loop for increasing a number of the high frequency clocks of the high frequency clock region; and

(c) an oscillator connected to the low frequency clock region.